江西欧云智能科技有限公司

JIANGXI OUYUN SMART TECH CO.,LTD.

液晶模组产品规格书

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Contents

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Change No.	**Date**	**Subject And Reason**	**Version No.**	**Responser**
1	2019.10.29	初版	00	

1.0 General Description

1.1 Introduction

HZ101HD220-31P is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel and a driving circuit.This TFT LCD has a10.1 inch diagonally measured active display area with (800 horizontal by1280vertical pixe l) resolution.

1.2. Features

10.1 inch configuration
ROHS design

1.3. General information

Item	Specification	Unit
Outline Dimension	143 (H) x 228.6(V) x2.6 (D)	mm
Display area	135.36 (H) x 216.567 (V)	mm
Number of Pixel	800 RGB (H) x1280 (V)	pixels
Pixel pitch	0.0564 (H) x 0.1692(V)s	mm
Pixel arrangement	Pixels RGB stripe arrangement	
Display mode	Normally Black	
Color Filter Array	RGB vertical stripes	
Backlight	White LED	
Weight	TBD	g
Data Transfer	MIPI	
Display colors	16.7 M	

2.0 Absolute Maximum Ratings

2.1 Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Operating Temperature	Topa	-10	50	℃	
Storage Temperature	Tstg	-20	60	℃	

2.2 Back-light Unit:

PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
LED Current	IF	–	200	–	mA	–	–
LED Voltage	VF	9.0	9.6	10.5	V	–	–
Life Time		–	20000	–	Hr.	I≦200mA	–
Color	White						

Note (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2)Ta=25±2℃

(3)Test condition: LED Current200mA

3.0 Optical Characteristics

3.1 Optical specification

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (CR≥ 10)	θ_L	Φ=180°(9 o'clock)		80	-	degree	
	θ_R	Φ=0°(3 o'clock)		80	-		
	θ_T	Φ=90°(12 o'clock)		80	-		
	θ_B	Φ=270°(6 o'clock)		80	-		
Response time	T_R+T_F	Normal θ=Φ=0°		20	35	msec	
						msec	
Contrast ratio	CR		600	800	-	-	
Color chromaticity	W_X		0.26	0.31	0.36	-	
	W_Y		0.28	0.33	0.38	-	
Luminance	L		200	250	-	cd/m²	
Luminance uniformity	Y_U		70	75	-	%	

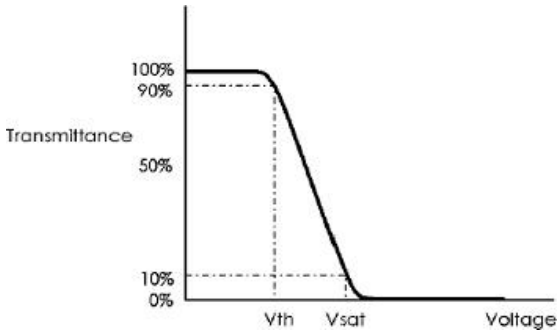
3.2 Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : 25±2℃
- 30min. warm-up time.

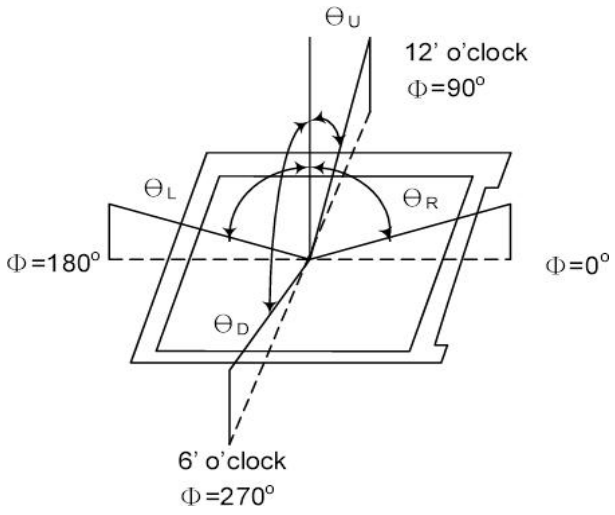
3.3 Measuring Equipment

- TOPCON BM-7
- Measuring spot size : field 2°

Note (1) Definition of Vsat and Vth (at 20℃)



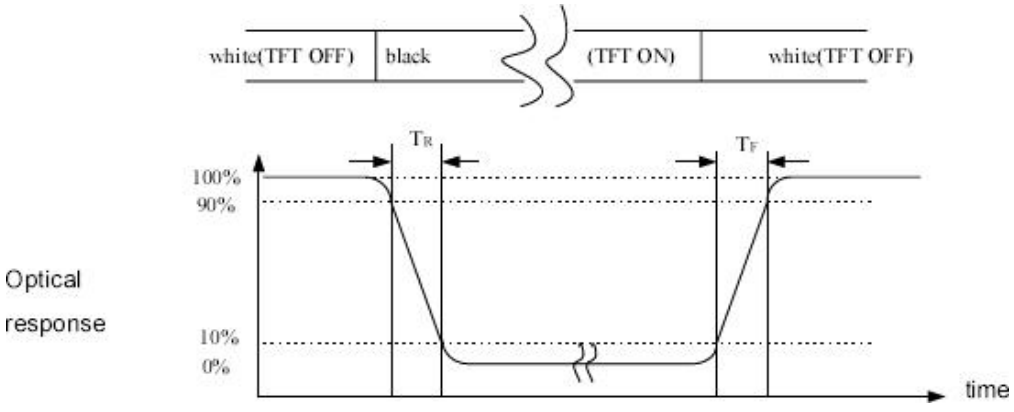
Note (2) Definition of Viewing Angle :



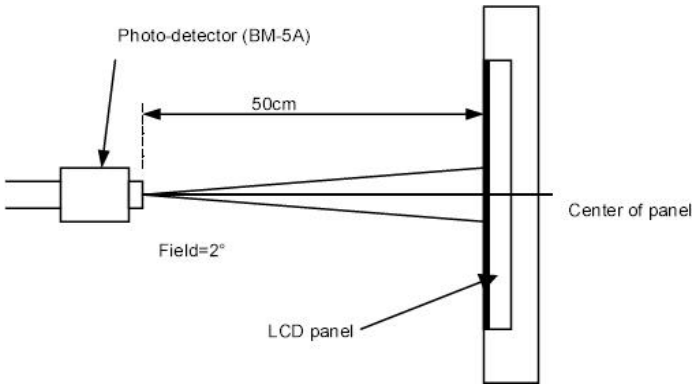
Note (3) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

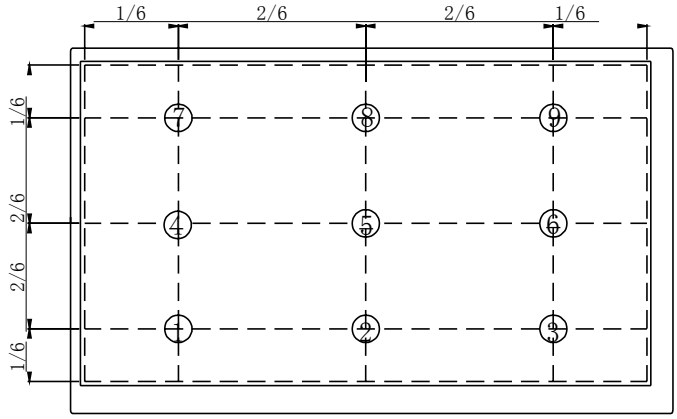
Note (4) Definition of Response Time : Sum of T_R and T_F



Note (5) Definition of optical measurement setup



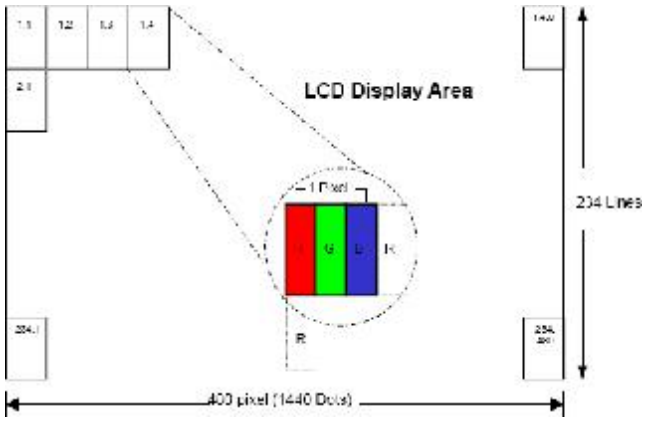
Note (6) Definition of brightness uniformity



Note (7) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.

4.0 Block Diagram

4.1 TFT-LCD Module



5.0 Interface Pin Connection

PIN NO	SYMBOL	DESCRIPTION
1	LEDA	Power for LED backlight(Anode)
2	LEDA	Power for LED backlight(Anode)
3	LEDA	Power for LED backlight(Anode)
4	NC	No connect
5	LEDK	Power for LED backlight(Cathode)
6	LEDK	Power for LED backlight(Cathode)
7	LEDK	Power for LED backlight(Cathode)
8	LEDK	Power for LED backlight(Cathode)
9	GND	Ground
10	GND	Ground
11	MIPI_D2+	HSSI_D2_Pare differential small amplitude signals
12	MIPI_D2-	HSSI_D2_Nare differential small amplitude signals
13	GND	Ground
14	MIPI_D1+	HSSI_D1_Pare differential small amplitude signals
15	MIPI_D1-	HSSI_D1_Nare differential small amplitude signals
16	GND	Ground
17	MIPI_CLK+	HSSI_CLK_Pare differential small amplitude signals
18	MIPI_CLK-	HSSI_CLK_Nare differential small amplitude signals
19	GND	Ground
20	MIPI_D0+	HSSI_D0_Pare differential small amplitude signals
21	MIPI_D0-	HSSI_D0_Nare differential small amplitude signals
22	GND	Ground
23	MIPI_D3+	HSSI_D3_Pare differential small amplitude signals
24	MIPI_D3-	HSSI_D3_Nare differential small amplitude signals
25	GND	Ground
26	NC	
27	RESET	Reset signal
28	NC	
29	VDD1V8	I/O power supply
30	VDD3V3	Power supply 3.0-3.6V
31	VDD3V3	Power supply 3.0-3.6V

6. Operation Specifications

6.1 Current Consumption

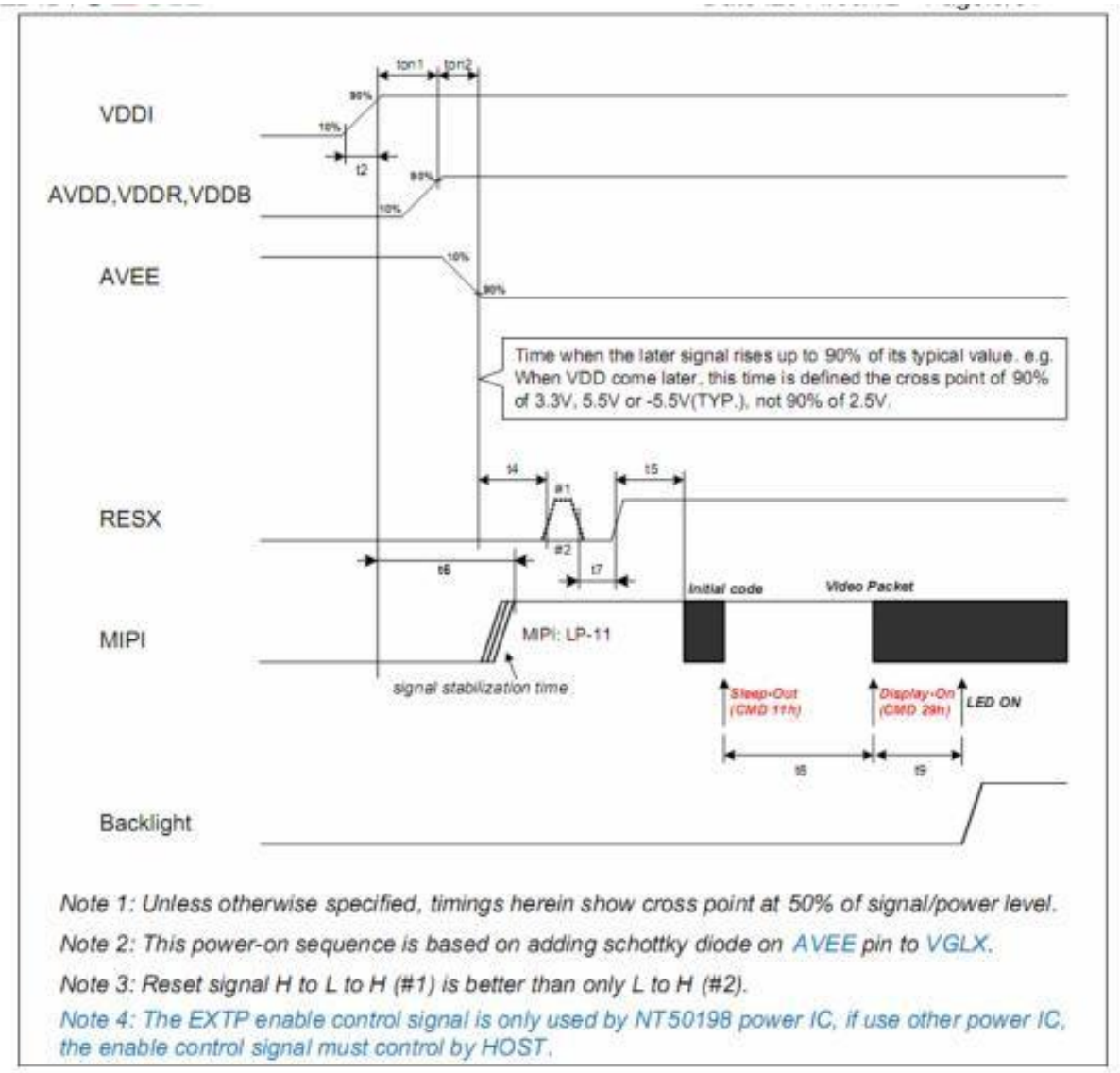
(GND=AV_{SS}=0V)

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Current for Driver	I_{VDDIN}		32	55	mA	
	I_{AVDD}		28	50	mA	
	I_{AVEE}		25	45	mA	

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.
Note (2) The specified power supply current is under the conditions at VDDI = 3.3 V, AVDD=5.8V,AVEE=-5.8,Ta = 25±2 ºC, DC Current and fv = 60 Hz

6.2 Power Seque

a. Power on:



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

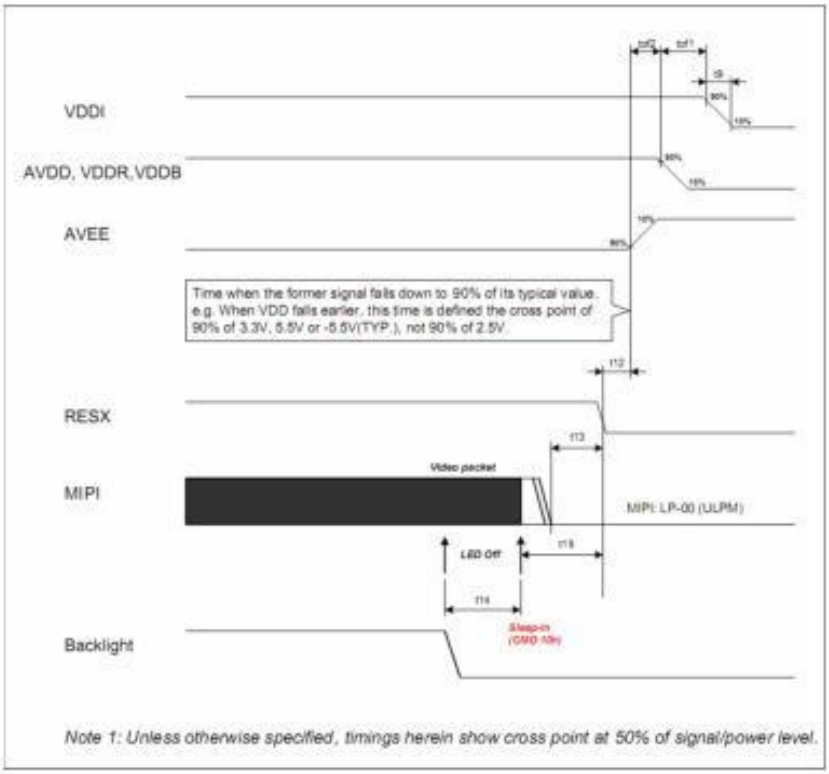
Note 2: This power-on sequence is based on adding schottky diode on AVEE pin to VGLX.

Note 3: Reset signal H to L to H (#1) is better than only L to H (#2).

Note 4: The EXTP enable control signal is only used by NT50198 power IC, if use other power IC, the enable control signal must control by HOST.

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1	0	-	-	ms	
ton2	0	-	-	ms	
ton3	0	-	-	ms	
ton4	0	-	-	ms	
t2	-	No limit	-	μs	
t4	10	-	-	ms	
t5	20	-	-	ms	
t6	0	-	t4	ms	
t7	10	-	-	μs	
t8	120	-	-	ms	
t9	0	No limit	-	vs	

b. Power off:



Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t9	150	-	-	μs	
tof1	0	-	-	ms	
tof2	0	-	-	ms	
tof3	0	-	-	ms	

tof4	0	-	-	ms	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	0	-	-	ms	
t15	100			ms	

6.3. MIPI interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

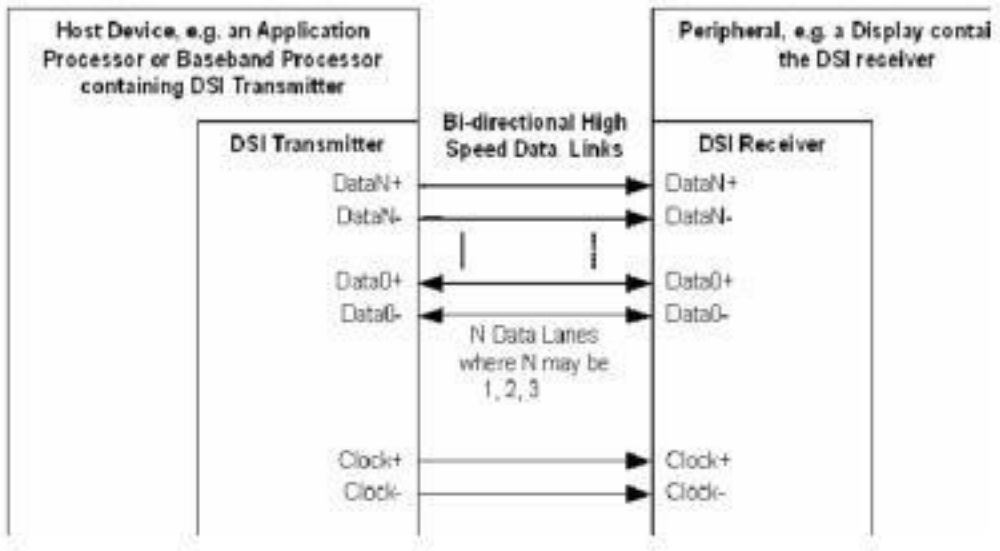
DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode.

Note: The product only supports Video Mode operation.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

	MCU (Master) Display Module (Slave)
Clock Lane+/-	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0+/-	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane1+/-	Unidirectional ■ Forward High speed
Data Lane2+/-	Unidirectional ■ Forward High speed
Data Lane3+/-	Unidirectional ■ Forward High speed

The connection between host device and display module is as reference.


Host Device, e.g. an Application Processor or Baseband Processor containing DSI Transmitter
DSI Transmitter
Bi-directional High Speed Data Links
Peripheral, e.g. a Display contai the DSI receiver
DSI Receiver
DataN+
DataN-
Data0+
Data0-
N Data Lanes where N may be 1, 2, 3
Clock+
Clock-

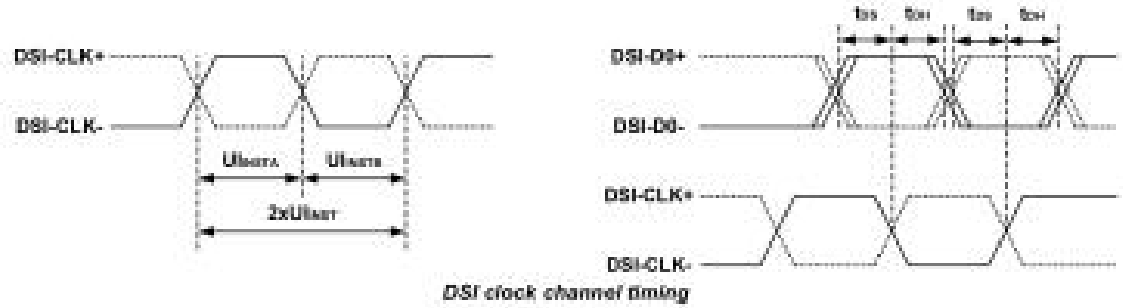
6.4. MIPI Signal Timing Characteristics

6.4.1. AC Electrical Characteristics

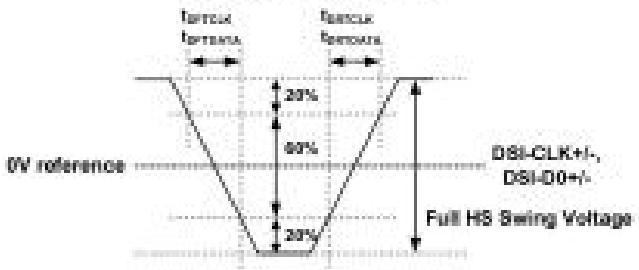
6.4.1.1 High Speed Mode

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	2xUIINST	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UIINSTA UIINSTB	UI instantaneous halfs (UI = UIINSTA = UIINSTB)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	tDS	Data to clock setup time	0.15x UI	-	-	ps	
DSI-Dn+/-	tDH	Data to clock hold time	0.15x UI	-	-	ps	
DSI-CLK+/-	tDRTCLK	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDRTDATA	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	tDFTCLK	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDFTDATA	Differential fall time for data	150	-	0.3xUI	ps	

Note 1) Dn = D0, D1, D2 and D3.
Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.
Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.



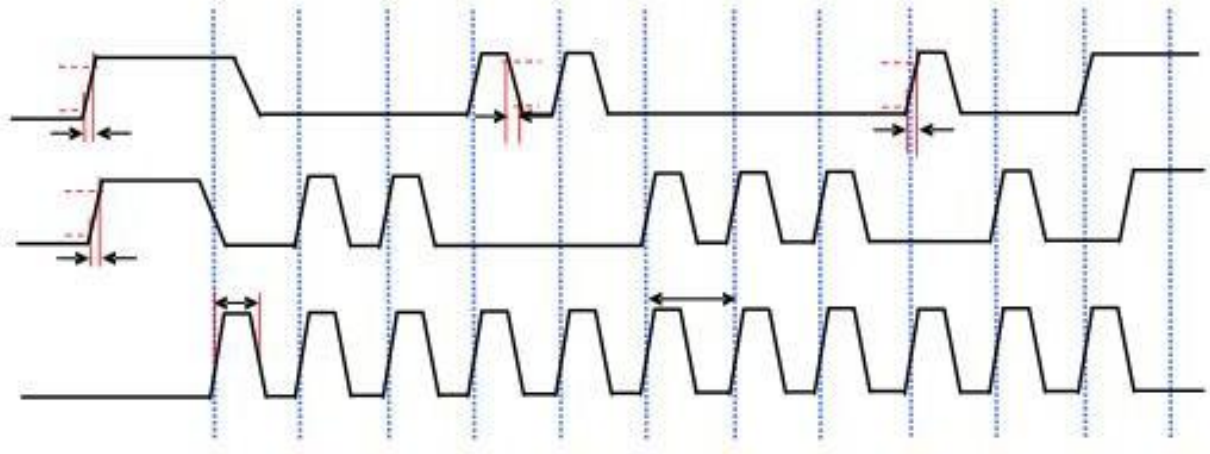
DSI clock channel timing



Rising and fall time on clock and data channel

6.4.1.2 LP Transmission

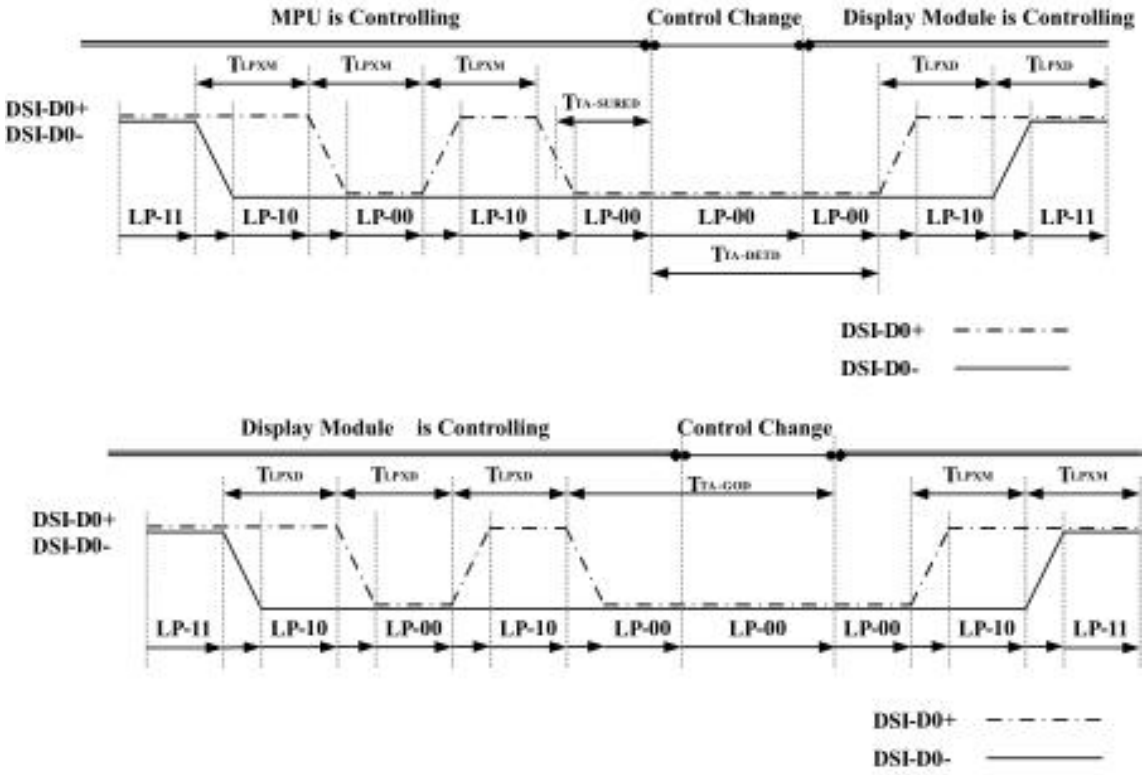
Parameter	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
DSI CLK frequency(LP)	F_{DSICLK_LP}			10	MHz	
DSI CLK Cycle Time(LP)	t_{CLKC_LP}	100			ns	
DSI Data Transfer Rate(LP)	t_{DSIR_LP}			10	Mbps	
15%-85% rise time and fall time	T_{RLP} / T_{FLP}	-	-	35	ns	
30%-85% rise time(from HS to LP)	T_{REOT}	-	-	35	ns	
Pulse width of the LP exclusive-OR clock	$t_{LP-PULSE-TX}$	50	65	-	ns	
Period of the LP exclusive-OR clock	$t_{LP-PRE-TX}$	100	130	-	ns	



6.4.1.3 Low Power Mode

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+ /-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU (Display Module	50	-	75	ns	Input
DSI-D0+ /-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (MPU	50	-	75	ns	Output
DSI-D0+ /-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2xTLPXD	ns	Output
DSI-D0+ /-	TTA-GETD	Time to drive LP-00 by display module	5xTLPXD	-	-	ns	Input
DSI-D0+ /-	TTA-GOD	Time to drive LP-00 after turnaround request - MPU	4xTLPXD	-	-	ns	Output

Bus Turnaround (BAT) from MPU to display module Timing



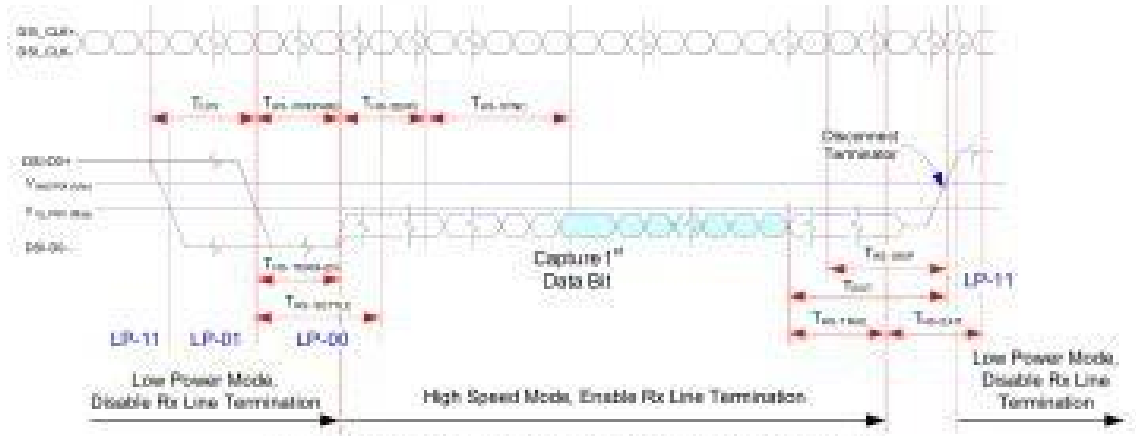
Bus Turnaround (BAT) from display module to MPU Timing

6.4.1.4 DSI Bursts

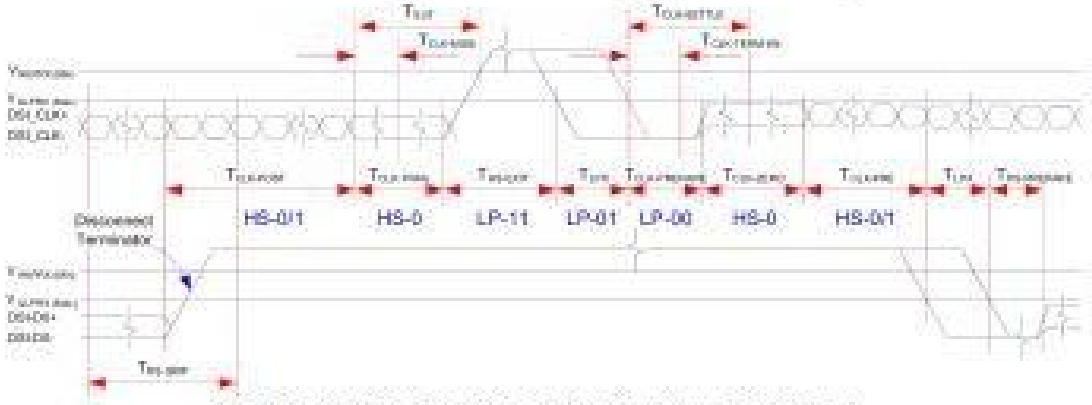
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to	60+52xUI	-	-	ns	Input

		LP mode					
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE+ TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.
Note 2) Two HS transmission can be sent with a break as short as THS-EXIT from each other in continuous clock mode. In discontinuous mode, the break is longer which account TCLK-POS, TCLK-TRAIL and THS-EXIT, before activity in clock and data lanes again.

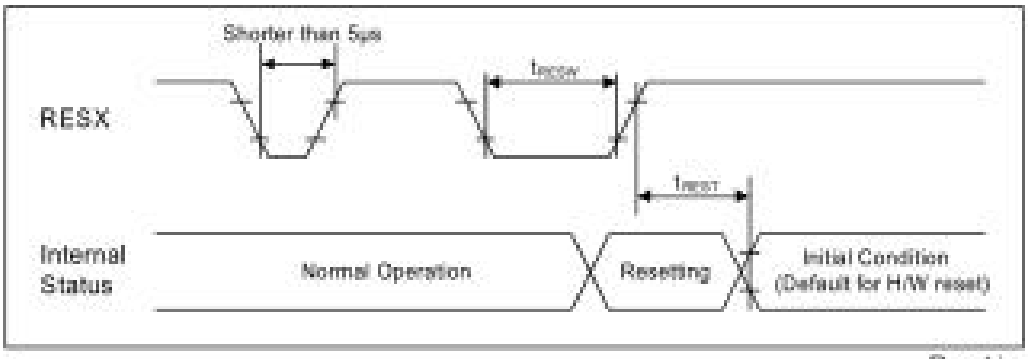


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

6.4.1.5 Reset Input Timing



Reset input timing
(VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t_{RESW}	Reset "L" pulse width (Note 1)	10	-	-	μs	
	t_{REST}	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset Start

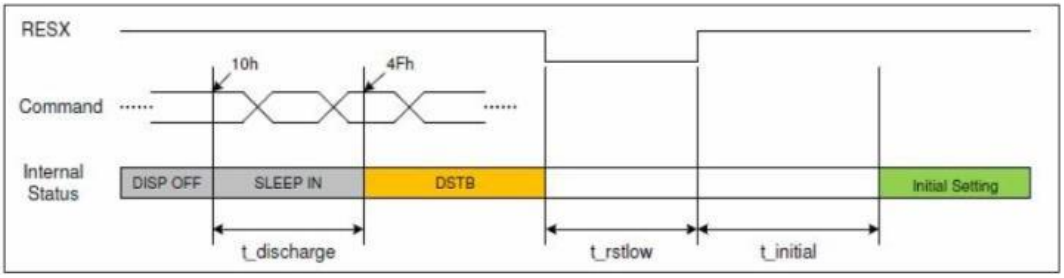
Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:

Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

6.4.1.6 Deep Standby Mode Timing



(***VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,***Ta = -30 to 70°C)

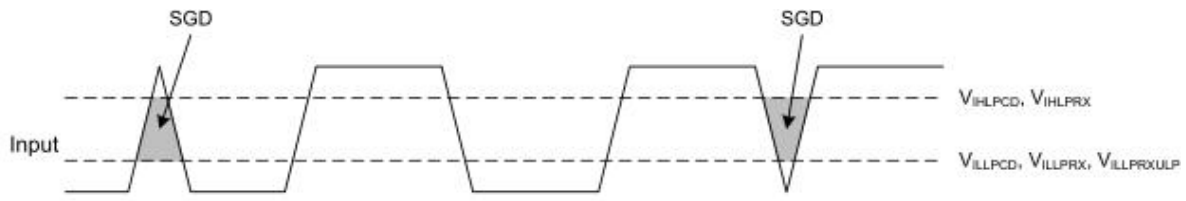
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tdischarge	Sleep in into DSTB delay time	-	-	100	ms	
	trstlow	Reset low pulse	3	-	-	ms	
	tinitial	Reset high to initial setting delay time	-	-	120	ms	

Note 1) t_discharge suggested delay time over 100ms.
Note 2) t_initial suggested delay time over 120ms..

6.4.2. DC Electrical Characteristics

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

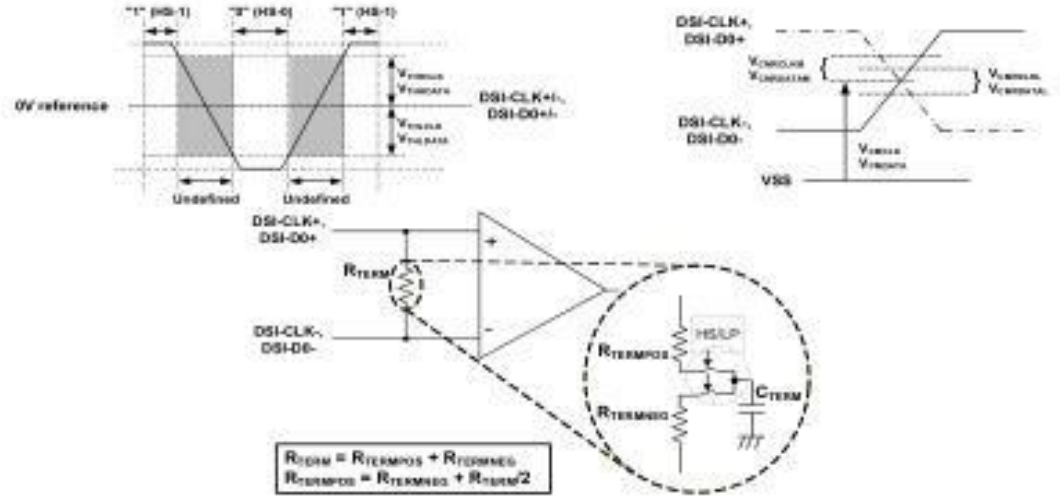
Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
Note 2) DSI high speed is off.
Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.



Spike/Glitch rejection-DSI

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	VCMCLK VCMDATA	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	VCMRCLKL VCMRDATAL	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	VCMRCLKM VCMRDATAM	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	VTHLCLK VTHLDATA	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	VTHHCLK VTHHDATA	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	VILHS	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	VIHHS	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	RTERM	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	VTERM-EN	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	CTERM	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 °C (to +85 °C no damage).
Note 2) Includes 50mV (-50mV to 50mV) ground difference.
Note 3) Without VCMRCLKM / VCMRDATAM.
Note 4) Without 50mV (-50mV to 50mV) ground difference.
Note 5) Dn=D0, D1, D2 and D3.



Differential voltage range, termination resistor and Common mode voltage

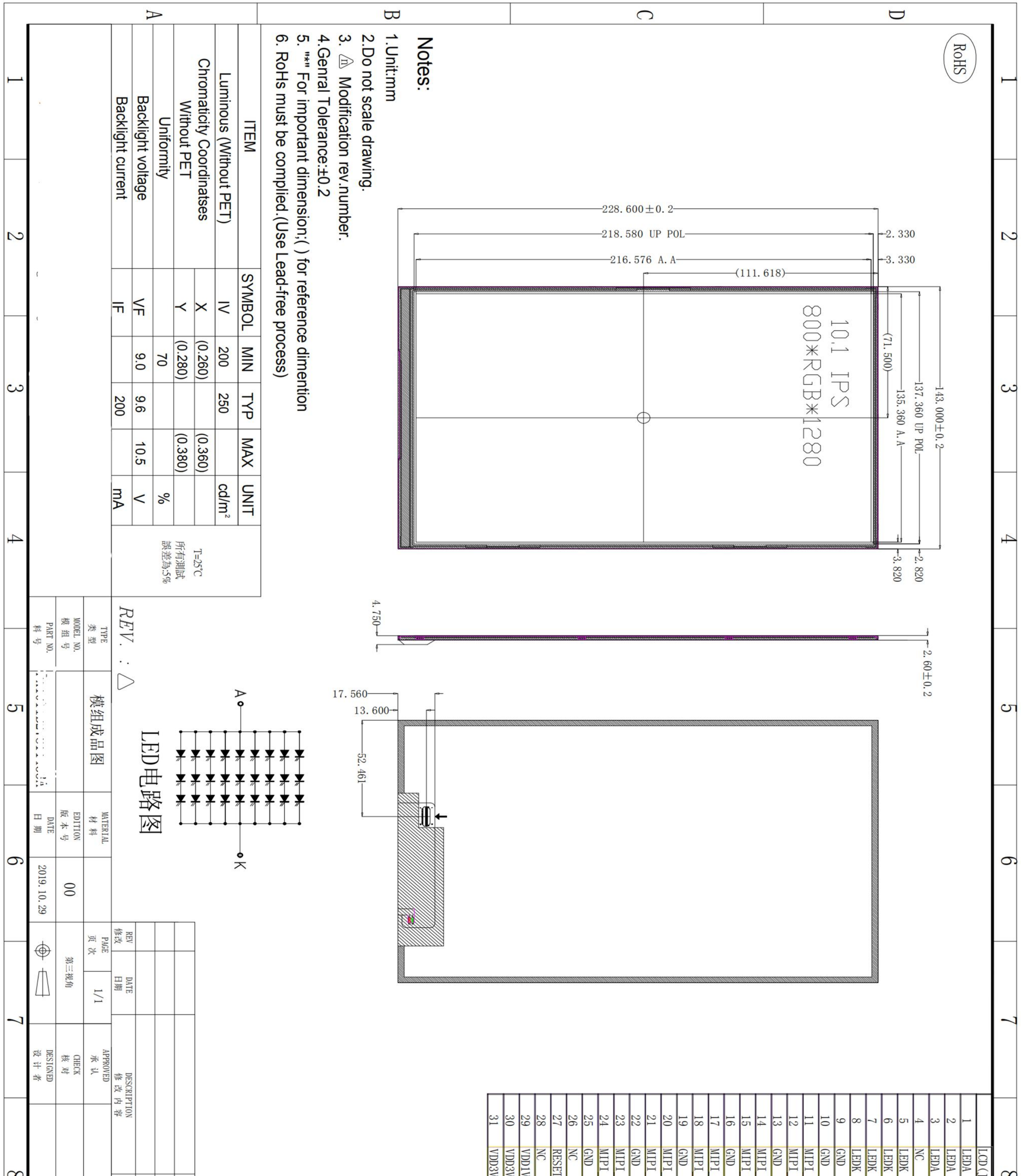
7.0 Reliability test items

NO	Item	Conditions	Remark
1	High Temperature Storage	Ta=+60℃,24hrs	
2	Low Temperature Storage	Ta=-20℃,24hrs	
3	High Temperature Operation	Ta=+50℃,24hrs	
4	Low Temperature Operation	Ta=-10℃,24hrs	
5	High Temperature and High Humidity (operation)	Ta=+40℃,90%RH,24hrs	
6	Thermal Cycling Test (non operation)	-20℃(0.5hr)→+60℃(0.5hr),100cycles	
7	Electrostatic Discharge	150pf/330Ω/±8KV air & contact test 200pf/0Ω/±4KV contact test	

Note: All tests above are practiced at module type.

There is no display function NG issue occurred, All the cosmetic specification is judged before the reliability stress.

8.0 Outline dimension



Notes:

1. Unit:mm
2. Do not scale drawing.
3. ⚠ Modification rev.number.
4. Genral Tolerance:±0.2
5. "*" For important dimension;( ) for reference dimention
6. RoHs must be complied.(Use Lead-free process)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	
Luminous (Without PET)	IV	200	250		cd/m²	T=25℃ 所有测试误差为5%
Chromaticity Coordinatses Without PET	X	(0.260)		(0.360)		
	Y	(0.280)		(0.380)		
Uniformity		70			%	
Backlight voltage	VF	9.0	9.6	10.5	V	
Backlight current	IF		200		mA	